Absolute Maximum Ratings

Symbol	Term	Value	Unit
V_S	Supply voltage prim.	18	V
V_{iH}	Input signal voltage (HIGH) max.	$V_S \pm 0,3$	V
I_{iH}	Input signal current (HIGH)	0,34	mA
I_{Gon}	Output current (peak) max.	3,3	A
I_{Goff}	Output current (peak) max.	3,3	A
$I_{outAVmax}$	Output average current SKHI21/SKHI22	+ 40[6]/± 20[6]	mA
V_{CE}	Collector-emitter voltage sense across the IGBTSKHI21/SKHI22	1200 / 1700	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	25 [1]	kV/µs
$V_{isol\ IO}$	Isolation test volt. IN-OUT (RMS; 1min.) input-output Version "H4": (1min.)	2500 4000	V~ V~
V_{isol12}	Isolation test voltage output 1-output 2 (RMS; 1min.)	1500	V~
T_{op}	Operating temperature	– 40 ... + 85	°C
T_{stg}	Storage temperature	– 40 ... + 85	°C

Electrical Characteristics

Symbol	Term	Value SKHI 21/ 22	Unit
V_S	Supply voltage primary side	15 ± 0,6	V
I_S	Supply current primary side max	160	mA
Iso	Supply current primary side no load	typ.75/typ.110	mA
V_{iT+}	Input threshold voltage (HIGH) min.	12,9	V
V_{iT-}	Input threshold voltage (LOW) max.	2,1	V
$V_{G(on)}$	Turn-on gate voltage output	15	V
$V_{G(off)}$	Turn-off gate voltage SKHI 21/SKHI 22	0/– 15	V
f	Operating frequency IGBT/MOS	→ page B14-28	
C_{ps}..	Coupling capacitances	see fig. 3	pF
$t_{d(on)\ io}$	Input-output turn-on propagation time	typ. 1 + t_{TD}	µs
$t_{d(off)\ io}$	Input-output turn-off propagation time	typ. 1	µs
$t_{d(err)}$	Error input-output propagation time	typ. 1	µs
V_{CEstat}	Reference voltage for V_{CE} monitoring [5]	typ. 6; max. 9	V

External Components see fig. 1 and fig. 4

Component	Function	Recommended value
R_{TD}	Dead time of interlock: $t_{TD}\,(\mu s) = 2,7 + 0,13 \cdot R_{TD}\,(k\Omega)$	0 [2] R_{TD} max.=100 kΩ
R_{CE}	Reference voltage for V_{CE} monitoring: $V_{CEstat}\,(V) = \frac{9 \cdot R_{CE}\,(k\Omega) - 25}{10 + R_{CE}\,(k\Omega)}$ (1)	R_{CE} = 24 kΩ min. 10 kΩ V_{CEstat} = 5,6 V max. 9 V
C_{CE}	Inhibit time for V_{CE} monitoring: $t_{min} = \tau_{CE} \cdot ln \left[\frac{15 - V_{CEstat}\,(V)}{10 - V_{CEstat}\,(V)} \right]$ (2) $\tau_{CE}(\mu s) = C_{CE}\,(nF) \cdot \frac{10 \cdot R_{CE}\,(k\Omega)}{10 + R_{CE}\,(k\Omega)}$ (3)	C_{CE} = 0,33 nF max. 2,7 nF t_{min} = 1,75 µs max. 10 µs τ_{CE} = 2,3 µs
R_{ON} R_{OFF}	Turn-on speed of the IGBT [3] Turn-off speed of the IGBT [4]	min. 3,3 Ω min. 3,3 Ω

SEMIDRIVER

Hybrid Double IGBT and MOSFET Driver SKHI 21, SKHI 21 H4 SKHI 22, SKHI 22 H4

Features

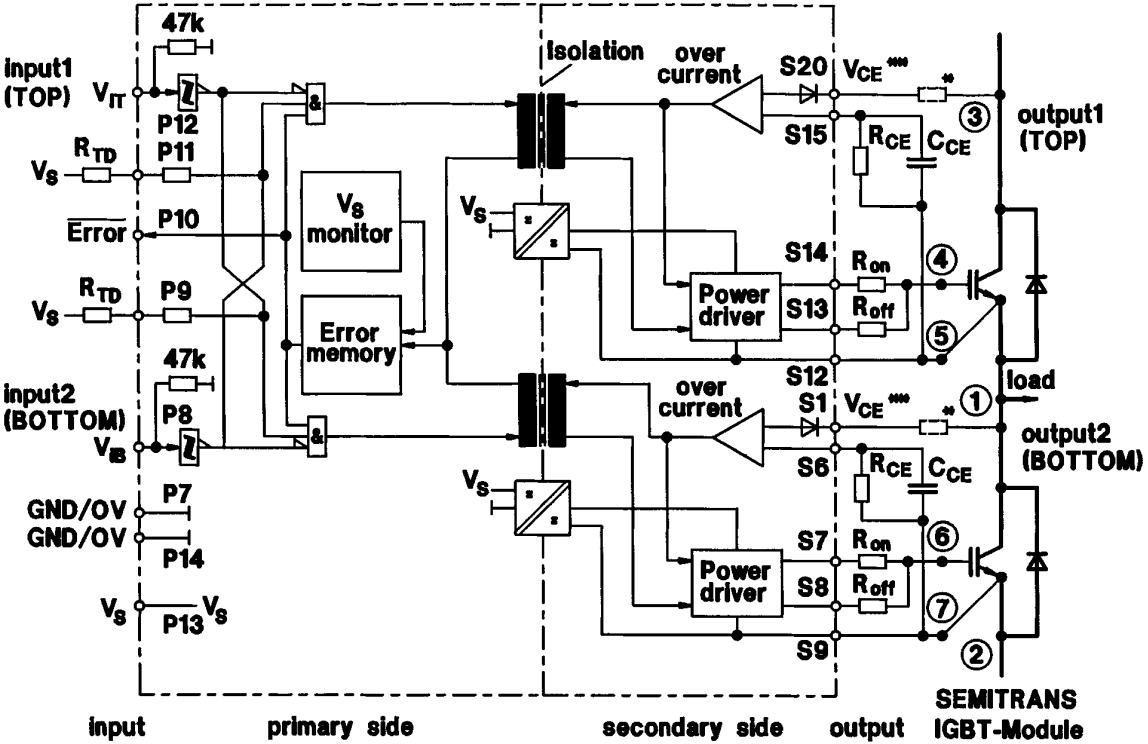
- Double driver for half bridge modules
- SKHI 22 H4 is for 1700 V-IGBT
- Drives MOSFETs $V_{DS(on)}$ < 10 V
- CMOS compatible inputs
- Short circuit protection by V_{CE} monitoring and switch off
- Drive interlock top/bottom
- Isolation by transformers
- Supply undervoltage protection (13 V)
- Error latch/output

Typical Applications

- Driver for IGBT and MOSFET modules in bridge circuits in choppers, inverter drives, UPS and welding inverters
- DC bus voltage up to 1000 V.

1) Primary/OUT2 = 10kV/µs +900 V
2) Short circuit for t_{TD} = 2,7 µs
3) Higher resistance reduces freewheeling diode peak recovery current, increases IGBT turn-on time. R_{ON} should be chosen so that the turn-on delay time $t_{d(on)}$ does not exceed 1 µs. See also Fig. 10
4) Higher resistance reduces turn-off voltage spike, increases turn-off time and turn-off power dissipation. See also Fig. 10.
5) adjustable by R_{CE}
6) double when using half driver

Blockdiagram SKHI 21; SKHI 22 Description of the Circuit



* When SKHI 22/H4 is driving 1700 V IGBTs, 1 kΩ / 0,4 W resistor must be added here to adjust internal voltage levels.

** This Terminal "V_{CE}" is to be connected to the IGBT collector. If the V_{CE} monitoring is not to be used, then connect S1 to S9 respectively S20 to S12.

Fig. 1 Block diagram of SKHI 21 and SKHI 22. The numbers refer to description see paragraph B, circled numbers to IGBT-terminals. Power output driver is a MOSFET type transistor pair, switching to V_{GE} = 0 V in type SKHI 21, respectively to V_{GE} = – 15 V in type SKHI 22.

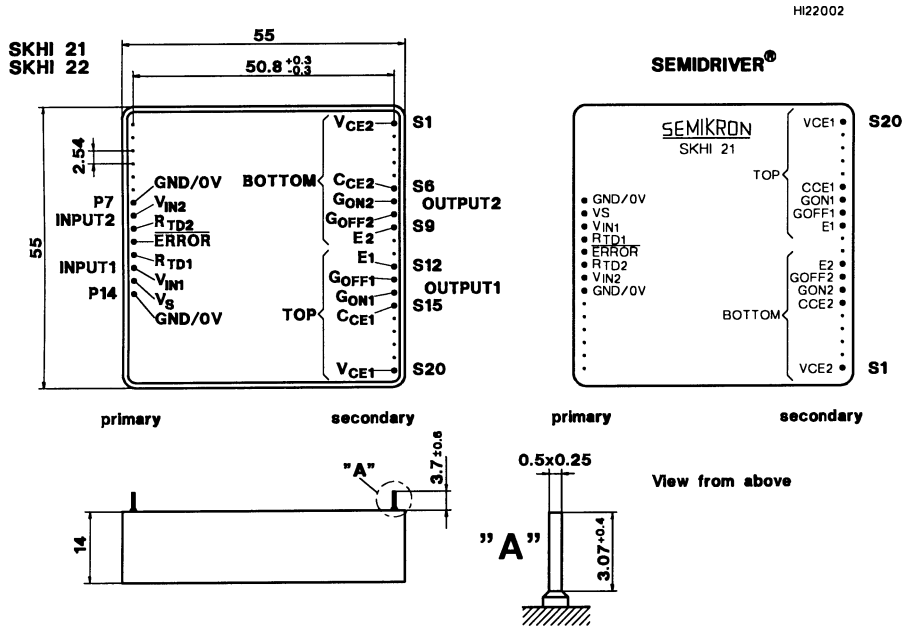
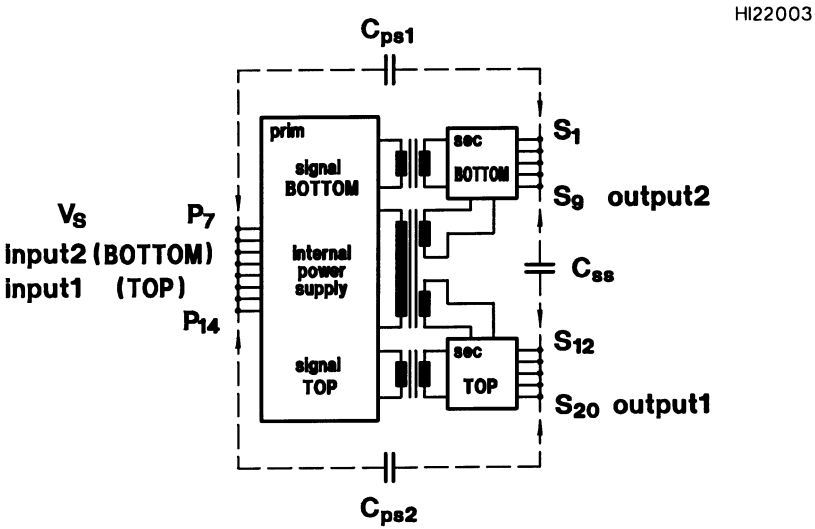


Fig. 2 Positions of the terminals (pin view) and dimensions (in mm). Weight: 55 g



C_{ps1}	primary to secondary 1 (TOP)	7,5 pF
C_{ps2}	primary to secondary 2 (BOTTOM)	7,5 pF
C_{ss}	secondary side (TOP to BOTTOM)	10 pF
C_{pstot}	total primary to secondary	15 pF

Fig. 3 Equivalent effective coupling capacitances, max. values.

SEMIDRIVER SKHI 21 and SKHI 22
Hybrid Double IGBT and MOSFET Driver
Technical Explanations

The following explanations apply to the use of the hybrid driver for power MOSFETs as well as for IGBTs. For the reason of brevity, in the following the IGBTs are mentioned only. Also the designations “collector” and “emitter” apply to IGBTs. For the MOSFETs “drain” and “source” are to be read instead.

A. Properties and Functions of the Hybrid Driver

1. The hybrid driver comprises the pulse generator as well as short circuit protection for two IGBTs in half bridge (pair of arms) connection. If a single IGBT or MOSFET is driven, output 1 is to be used, and the terminal V_{CE2} (S1) of output 2 is to be connected to terminal E_2 (S9).
2. It may also be used for two power MOSFETs in half bridge connection, provided the drain-source voltage in the on-state does not exceed 10 V.
3. Short circuit protection is provided by measuring the collector-emitter voltage, turns “error” (pin P10) to “Low” < 0,7 V (I sink ≤ 4 mA).
4. The heatsink temperature may be monitored by a bimetal thermal trip connected between P10 “error” and “GND”. It turns on, when the rated temperature is exceeded. Carefully regard the isolation voltage of the bimetal trip contacts and the different ground potentials of heatsink and pcb’s.
5. The IGBTs are turned on by applying a positive gate-emitter voltage of 15 V, and turned off by connecting (SKHI 21)the gate with the emitter or (SKHI 22) with – 15 V against the emitter (pin S12 resp. S9). The gate is low-ohmic connected with the emitter as long as the IGBT has to remain in the off-state and as long as the supply voltage is present. In case of a failure of the supply voltage the gate-emitter connection is provided by a 22 kΩ resistor.
6. The hybrid driver comprises the auxiliary power supplies for the two boosters which are isolated by DC/DC converters.
7. The two IGBTs of the half bridge are interlocked in order to prevent them from being in the on-state simultaneously. The locking time between the turn-off signal for one IGBT and the release of the turn-on signal for the other one is typically 2,7 µs (> t_{doff}). It may be prolonged by external resistors: R_{TD}.
8. In the case of a short circuit both IGBTs are turned off immediately. An error memory prevents the IGBTs from being turned on again. The status of this memory may be fed back to the control circuit ($\overline{error}$ signal). The $\overline{error}$ memory is reset only when both input signals are zero. The error signal is provided by an open collector stage at pin 10 with an internal pull-up resistor of 10 kΩ to V_S. Parallel connection of $\overline{error}$ signal outputs is possible.
9. The nominal voltage of the power supply V_S is +15 V. Its band of variation is from 14,4 to 15,6 V. The current required is lower than 160 mA (conditions: 85 °C temperature, V_S = 15 V. Any undervoltage below +13 V is monitored, and the IGBTs are turned off. An error signal is released. Overvoltage is not monitored. (See page B 14 – 28).
10. The switching signals are transmitted by isolating pulse transformers. The isolation test voltages are $V_{isol\ IO}$ and V_{isol12}, abs. max. ratings see page 1. Versions “H4" have $V_{isol\ IO}$ = 4,0 kV_{RMS}.

    The max. dv/dt rating between primary and secondary side is 25 kV/µs (Primary/OUT 1) and 10 kV/µs + 900 V (Primary/OUT 2).
11. The input and output signals are CMOS compatible. The inputs have a Schmitt trigger characteristic to suppress spurious pulses. Turn-on and turn-off pulses shorter than 0,5 µs are not transmitted. The thresholds of the inputs are

    V_T^+ = min. 12,9 V
    V_T^- = max. 2,1 V
12. The maximum pulse frequency is 100 kHz (for MOS)
13. The operating temperature range is – 40 ... + 85 °C.
14. The typical delay times and propagation times for signals are

Turn-on:	1 µs + t_{TD}	input to output
Turn-off:	1 µs	input to output
Error:	1 µs	error input to error signal output

15. In order to optimize the turn-on and turn-off speeds external resistors may be connected according to the conditions of the given application.
16. The collectors of the IGBTs are connected to the hybrid driver for monitoring the collector-emitter voltage V_{CE}.
17. The required inhibit time t_{min} of the V_{CE} monitoring is to be matched to the turn-on speed of the IGBT. The standard setting with the recommended external components R_{CE} = 24 kΩ and C_{CE} = 330 pF is τ_{CE} = 2,3 µs. It may be increased by an external capacitor. The threshold voltage may be set by the external resistor R_{CE} up to maximum < 10 V.

B. Description of the Circuit Block Diagram

The circuit block diagram (Fig. 1) shows the input on the left and the output on the right.

The input side comprises the following components:

1. **Input Schmitt trigger, CMOS compatible**

2. **Interlock circuit**

   The interlock circuit prevents the IGBT to turn on before the gate charge of the other IGBT is completely discharged. It is to be set to a delay time longer than the turn-off time of the IGBT by two external resistors R_{TD} (maximum permissible value 100 kΩ) connected to the terminals R_{TD} and V_S. The delay time t_{TD} is typically:

   $$t_{TD}\,(\mu s) = 2{,}7 + 0{,}13 \cdot R_{TD}\,(k\Omega) \qquad (4)$$

   See also Fig. 5.

3. **Short pulse suppression**

   With very short turn-on or turn-off pulses the pulse transformer would be not completely re-magnetized, and the coupling capacitor at the input of the pulse transformer would be not completely re-charged. As a result, the flip-flop at the output of the driver would remain in the wrong state due to the unsufficient trigger pulse. The short pulse suppression makes sure that only adequate trigger pulses are transmitted to the output flip-flop.

4. **Error monitoring**

   This circuit monitors pulses fed backwards via the pulse transformers.

5. **Inhibit pulse generator**

   In the error monitoring circuit, an inhibit pulse generator discriminates between switching and error signals. After any positive switching pulse edge the error monitoring function is enabled. This is required since the pulse transformer causes a negative peak voltage on its primary during re-magnetization. This peak voltage would trigger the error monitoring without the inhibit pulse.

6. **Error memory**

   The error memory is triggered by the error monitoring circuit. The error memory blocks the turn-on pulses to both IGBTs simultaneously. Resetting is only possible when no pulses from the error monitoring are present and both inputs (on/off) are zero. The output signal is fed to a terminal which is to be connected to the control circuit.

7. **1 MHz Oscillator**

   It is the primary side control of the DC/DC converter for transmitting the control power to the IGBTs.

8. **Power supply monitoring**

   The supply voltage V_S is monitored for its minimum value of 13 V. If it falls below this value an error is monitored and the turn-on pulses for the IGBTs are blocked.
   At initial switch-on (VS) the input pulses may only be released more than 4 µs after the instant when V_S has reached its nominal value of 15 V.

The output comprises two drivers with the following components:

9. **Pulse transformer**

   It transmits the turn-on and turn-off signals for the IGBT. In the reverse direction the error signal from the V_{CE} monitoring is transmitted via the same transformer.

10. **Power supply transformer for the DC/DC converter**

11. **Rectifier for the auxiliary power supply**

12. **Flip-flop**

    The flip-flop is pulse width triggered and is insensitive to spurious pulses and high dv/dt values.

13. **Drivers**

    The output transistors of the power drivers are MOSFETs.
    The sources of these MOSFETs are connected to external terminals in order to provide the setting of the turn-on and turn-off speed by the external resistors R_{ON} and R_{OFF}. Do not connect the terminals S7 with S8, respectively S13 with S14, and use both, R_{on} and R_{off}, to avoid spurious switch-on effects.

14. **Reverse drivers for the pulse transformers**

    They transmit the signals from the V_{CE} monitoring to the pulse transformers.

15. **V_{CE} monitoring**

    It monitors the collector-emitter voltage V_{CE} of the IGBT during its on-state. V_{CE} is limited internally to 10 V (see fig. 4).

    If the reference voltage V_{CEref} is exceeded, the output signal switches to zero. V_{CEref} is dynamic. Immediately after turn-on of the IGBT a higher value is effective than in the steady state. When the IGBT is turned off, V_{CEref} is set to this higher value by the signal “reset”. The steady-state value V_{CEstat} of V_{CEref} is set for each IGBT by an external resistor R_{CE} (connected to the terminals C_{CE} and E) to the required maximum value (which may not exceed 10 V).

    V_{CEstat} as a function of R_{CE} is approximately:

    $$V_{CEstat}\,(V) = \frac{9 \cdot R_{CE}(k\Omega) - 25}{10 + R_{CE}\,(k\Omega)} \qquad (1)$$

    The time constant for the delay of V_{CEref} may be increased by an external capacitor C_{CE}, which is connected in parallel to R_{CE}. It controls the time t_{min} which passes after turn-on of the IGBT before the V_{CE} monitoring is activated. After t_{min} the V_{CE} monitoring functions immediately when V_{CEref} is exceeded.

    The standard setting with the external components R_{CE} = 24 kΩ and C_{CE} = 330 pF is t_{min} = 1,75 µs.

    $$t_{min} = \tau_{CE} \cdot \ln\left[\frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}\,(V)}\right] \qquad (2)$$

    $$\tau_{CE}\,(\mu s) = C_{CE}\,(nF) \cdot \frac{10 \cdot R_{CE}\,(k\Omega)}{10 + R_{CE}\,(k\Omega)} \qquad (3)$$

    V_{CEstat} is the value given by equation (1).

The required values of R_{CE} and C_{CE} are determined in four steps

1. Choose V_{CEstat} — see Fig. 9
2. Calculate R_{CE} from equation (1): $R_{CE} > 10\ k\Omega$
3. Choose t_{min} (2) $t_{min} < 10\ \mu s$
4. Calculate C_{CE} from equation (2) and (3).

Typical values are:

$R_{TD} = 0$, $R_{CE} = 24\ k\Omega$, $C_{CE} = 330\ pF$, $V_{CEstat} = 5{,}6\ V$; inhibit time for V_{CE} monitoring: $t_{min} = 1{,}75\ \mu s$

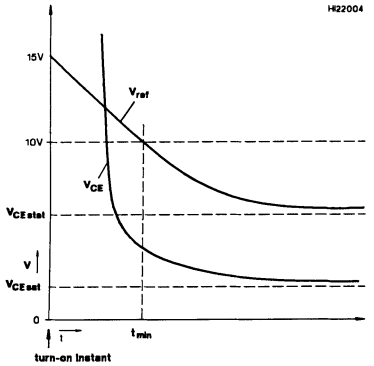


Fig. 4 Waveform of the reference voltage V_{CEref} of the V_{CE} monitoring immediately after the turn-on signal for the IGBT. A possible waveform of V_{CE} is shown. V_{CE} is internally clamped to 10 V.

C. Terminal Configuration

Fig. 2 shows the configuration of the terminals. The input comprises eight terminals, forming the interface to the control circuit. See also Fig. 1.

The output shows two symmetric groups of terminals for the connections to the two IGBTs.

The arrangement of the pins is shown in the figures 1 and 2. The distance between two groups is appropriate for the isolation test voltage of $V_{rms} = 1{,}5\ kV$, applied for 1 min. The grid is 2,54 mm (0,1").

D. External components

Fig. 1 shows the required external components which are all needed twice:

R_{TD} = Resistor for setting the delay time for the interlock
$t_{TD}\ (\mu s) = 2{,}7 + 0{,}13 \cdot R_{TD}\ (k\Omega)$ (4)
R_{TD} max = 100 kΩ

R_{CE} = Resistor for setting the threshold V_{CEstat} for the V_{CE} monitoring (see equation (1)).
R_{CE} min = 10 kΩ

C_{CE} = Capacitor for setting the delay time for the V_{CE} monitoring after turn-on of the IGBT (see equations (2) and (3)).
C_{CE} max = 2,7 nF

R_{ON} = Resistor for setting the turn-on speed of the IGBT. With a higher R_{ON} the turn-on speed is decreased, and the peak reverse recovery current of the free-wheeling diode is reduced.

It is recommended to choose R_{ON} such that the turn-on delay time of the IGBT remains below 1 µs.
R_{ON} min = 3,3 Ω

R_{OFF} = Resistor for setting the IGBT's turn-off speed. With a higher R_{OFF} the turn-off is slower, and the voltage spike across the parasitic inductances is reduced.
R_{OFF} min = 3,3 Ω

E. Signal Waveforms, Frequency Limits

The permissible ambient temperature range is – 40 to + 85 °C.
The following signal waveforms were observed under the following conditions: $V_S = 15\ V$ and $T_{amb} = 25\ °C$. All times are typical values if not otherwise specified.

Fig. 5 shows a normal signal waveform and standard delay times between input and output.

The switching thresholds V_T^+ und V_T^- of the input signal are

On: "High" V_T^+ = min. 12,9 V
Off: "Low" V_T^- = max. 2,1 V

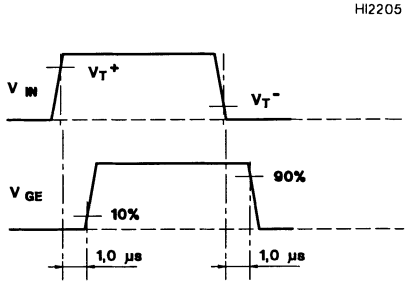


Fig. 5 Delay times during turn-on and turn-off of an IGBT.
V_{IN} = Input signal
V_{GE} = Output voltage of the hybrid driver with the terminals G_{ON} and G_{OFF} connected. Conditions for the above switching waveforms are: no error, the second input signal remains zero and $R_{TD} = 0$.

Fig. 6 (see page B 14 – 27) shows the function of the drive interlock with simultaneous change of the two input signals a delay takes place for the IGBT to be turned on which prevents a short circuit current to flow through the two power switches of the half bridge circuit. This delay time may be prolonged by a resistor R_{TD}. See the section on "the external components" and equation (4).

With turn-off signal 1 and turn-on signal 2 appearing simultaneously, the turn-on output signal is delayed by t_{TD}. At $R_{TD} = 0$, $t_{TD} = 2{,}7\ \mu s$. With $R_{TD} > 0$, t_{TD} is increased.

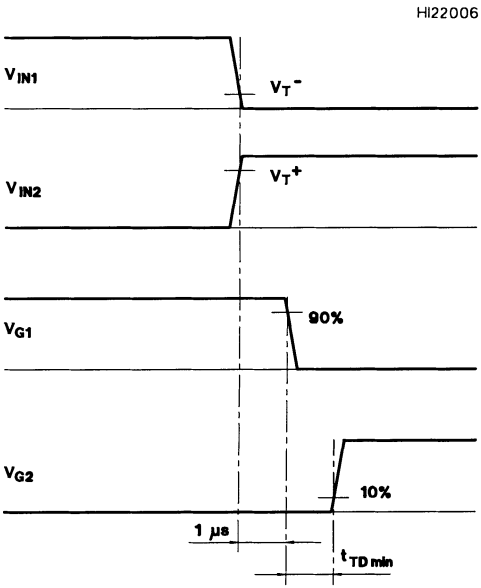


Fig. 6 Function of the drive interlock.

In Fig. 7 the V_{CE} monitoring is activated immediately after turn-on. t_{min} is the delay time according to equation (2). The value t_{min} = 1,75 µs is set using R_{CE} = 24 kΩ and C_{CE} = 330 pF.The signal waveforms in Fig. 7 from the instant S of activation of the V_{CE} monitoring on are also valid in case that the short circuit at the power switch happens some time after turn-on (S = instant of the short circuit = instant of activation of the V_{CE} monitoring $V_{CE} > V_{CEref}$).

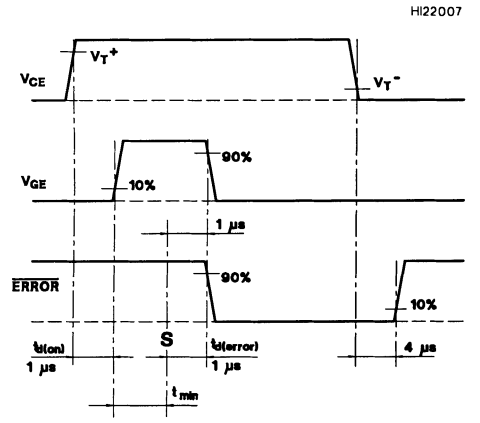


Fig. 7 Function of the short-circuit protection.
t_{min} = 1,75 µs for R_{CE} = 24 kΩ and C_{CE} = 330 pF.

F. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than (V_S + 0,3 V) or under - 0,3 V may destroy these inputs.

   Therefore the following safety requirements are to be observed:

   - To make sure that the control signals do not comprise overvoltages exceeding the above values.
   - Protection against static discharges during handling. As long as the hybrid driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be statically chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded.
     The same safety requirements apply to the IGBTs and power MOSFETs.

2. The connecting leads between the driver and the power module must be as short as possible.

   For MOSFETs and IGBT the leads should be twisted.

3. Any parasitic inductances should be minimized. Overvoltages may be damped by C or RCD snubber networks between the main terminals ③ = C 1 (+) and ② = E 2 (–) of the power module.

4. When first operating a newly developed circuit, low collector voltage and load current should be used in the beginning, and these values should be increased gradually, observing the turn-off behaviour of the free-wheeling diodes and the turn-off voltage spikes across the IGBT by means of the oscilloscope. Further the case temperature of the power module should be monitored. When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.

5. It is important to feed any errors back to the control circuit and to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short circuit with a frequency of several kHz may destroy the device.

6. Mechanical fixing on PCB:
   In applications with mechanical vibrations or shock, especially in vehicle applications – do not fix the SEMIDRIVER on a printed circuit board (PCB) by a ty-rap. But – after soldering and testing – you may apply a bead of special glue (proposed types: CIBA GEIGY XP 5090 + 5091;
   PACTAN 5011; WACKER A33 (ivory) or N199 (transparent), around the case edge, to fix it mechanically to PCB. Do not press the case and do not twist the PCB with SEMIDRIVER soldered on.
   The internal ceramic may crack. It is not suitable for a big PCB. Small PCB are available, see page 8.
   Tested acceleration (x; y; z-axis):
   10 – 100 Hz: 1,5 x g; shock: 5 x g
   (TÜV as per LES-DB-BN 411002)

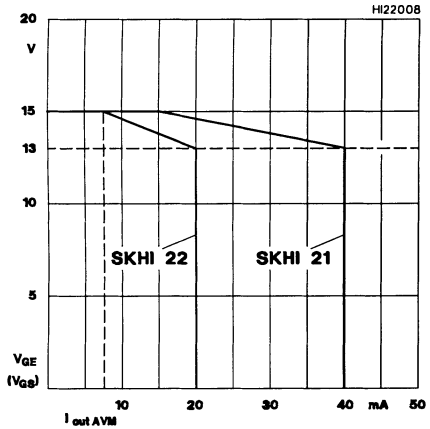


Fig. 8 Output characteristic: voltage V_{GE} vs. allowable average output current I_{outAV} of each channel

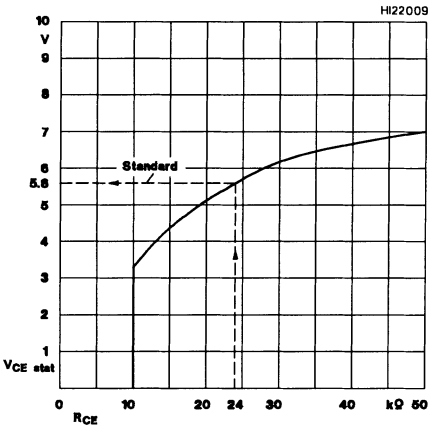


Fig. 9 V_{CEstat} as a function of R_{CE} (kΩ)

The frequency limit of driving by SKHI 21 or SKHI 22 is achieved, when the output voltage V_{GE} = 13 V (or V_{GS} = 10 V using MOSFET).
The maximum switching frequency for IGBTs f_{max} can be calculated as follows:
For SKHI 21 with Q_{gel} at V_{GE} = 13 V:

$$f_{max} = \frac{I_{outAVmax}(mA) \cdot 10^3}{Q_{gel}(nC)}\ (kHz);\ \text{with } I_{outAVmax} = 40\ mA \quad (5)$$

For SKHI 22 with Q_{gel} at V_{GE} = 13 V (due to the double voltage range – 15 V / + 15 V):

$$f_{max} = \frac{I_{outAVmax}(mA) \cdot 10^3}{2 \cdot Q_{gel}(nC)}\ (kHz);\ \text{with } I_{outAVmax} = 20\ mA \quad (5)$$

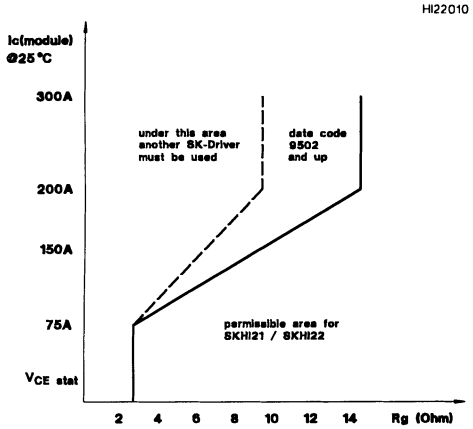


Fig. 10 R_{gon} (and R_{goff} for SKHI 22) minimum value valid for 1200 V-IGBT

A printed circuit board (PCB) type SKPC 2006 (**) to carry a SEMIDRIVER SKHI 21 or SKHI 22. → page B 14 – 20 and – 37
The PCB contains the necessary tracks to connect the external capacitors and resistors to the semidriver as mentioned in Fig. 1.
This unit can directly be plugged on to the SEMITRANS-3 IGBT module and be fixed to the heatsink by 3 bolts.
Dimensions: L x W x H = 96 x 67 x 1,5 mm.

(*) 80 mA when using only half driver (**one** single module).
(**) can be ordered

No. 11220040

SEMIDRIVER SKHI 22 on PCB SKPC 2006

